```
----- lcd.vhd -----
--*****************************************
--
--  PLD for LCD unit  ver 1.0
--
--  programmed by kaneko  Jan.5 2005
--
--*****************************************
library ieee;
use ieee.std_logic_1164.all;

--=========================================
--
--  entity
--
--=========================================
entity lcd is
    port(
        ----- CPU side -----
        CS1n    : in    std_logic;                      -- chip select 1
        CS2n    : in    std_logic;                      -- chip select 2
        AB0     : in    std_logic;                      -- address bus
        RDn     : in    std_logic;                      -- read pulse
        WRn     : in    std_logic;                      -- write pulse
        DB      : inout std_logic_vector(7 downto 0);   -- data bus
        ----- LCD side -----
        RS      : out   std_logic;                      -- register select
        RW      : out   std_logic;                      -- read/write select
        E       : out   std_logic;                      -- enable pulse
        LDB     : inout std_logic_vector(7 downto 0)    -- LCD data bus
        );
end lcd;

--=========================================
--
--  architecture
--
--=========================================
architecture RTL of lcd is
begin
    ----- make control signal -----
    RS <= AB0;
    RW <= WRn;
    E <= '1' when CS1n = '0' and CS2n = '0' and (RDn = '0' or WRn = '0') else
         '0';

    ----- make LCD data bus -----
    LDB <= DB when CS1n = '0' and CS2n = '0' and WRn = '0' else
           (others => 'Z');

    ----- make CPU data bus -----
    DB <= LDB when CS1n = '0' and CS2n = '0' and RDn = '0' else
          (others => 'Z');

end RTL;
```