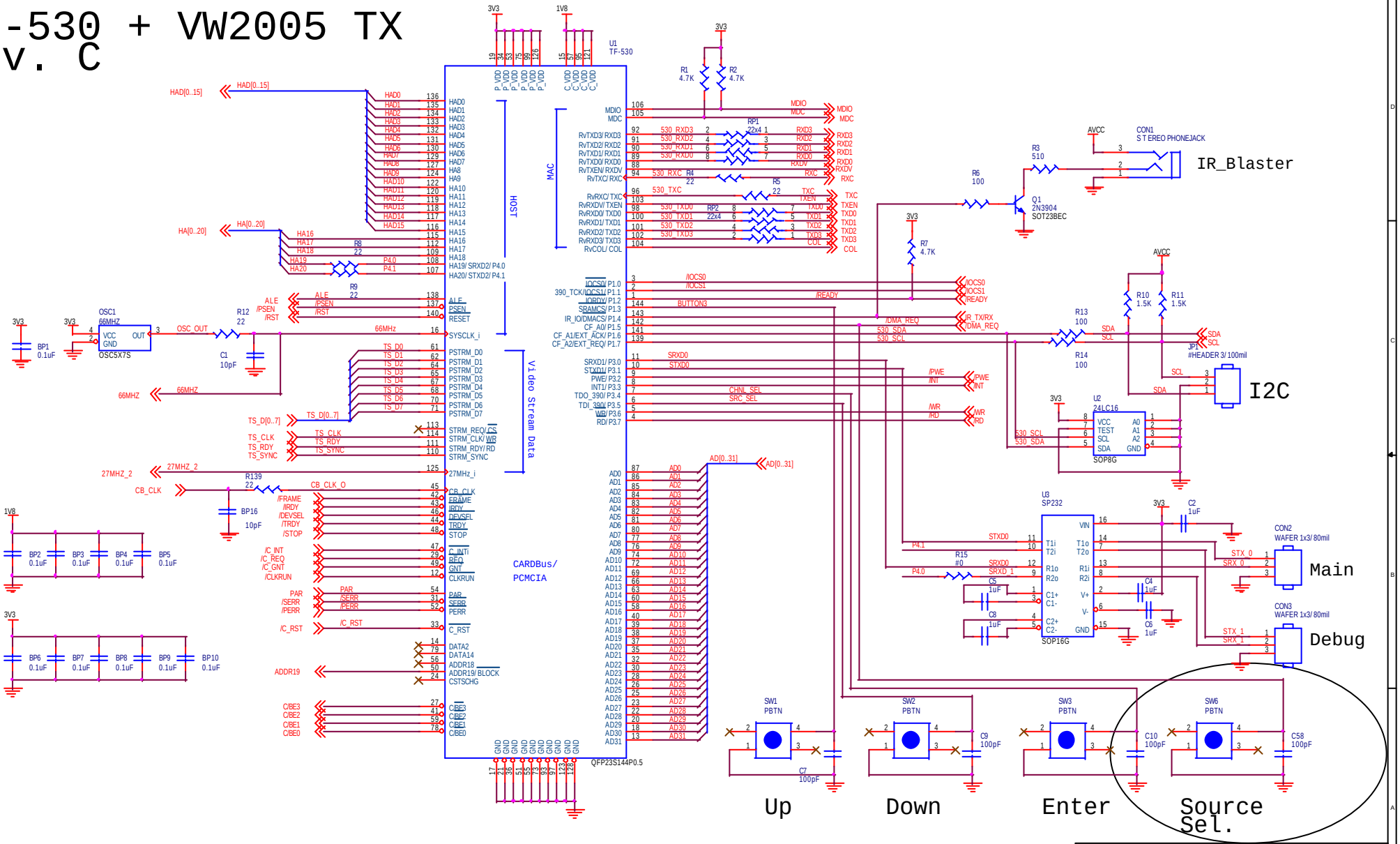
# TF-530+VW2005 TX

| Date MM/DD/YY | Revision | Description | By |
|---|---|---|---|
| 01/14/04 | A | First Release. | Chance |
| 04/21/04 | B | 1. Add Flip-Flop to Card-bus.<br>2. Change VW2010's HIF to Motolora mode.<br>3. Add one more address latch (High Addr.).<br>4. Add one PLD/ 16V8 for glue-logic | Chance |
| 08/17/04 | C | 1. Change Card-bus to Mini-PCI<br>2. Change PHY to ADM7001<br>3. Modify WLAN's power circuitry<br>4. Add A/V input circuitry and Tuner<br>5. Add A/V decoder SAA7173<br>6. Change to VW2005 | Chance |

# TF-530 + VW2005 TX Rev. C

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| | | |
|---|---|---|
| Title | TF-530 + VW2005: TF-530 | |
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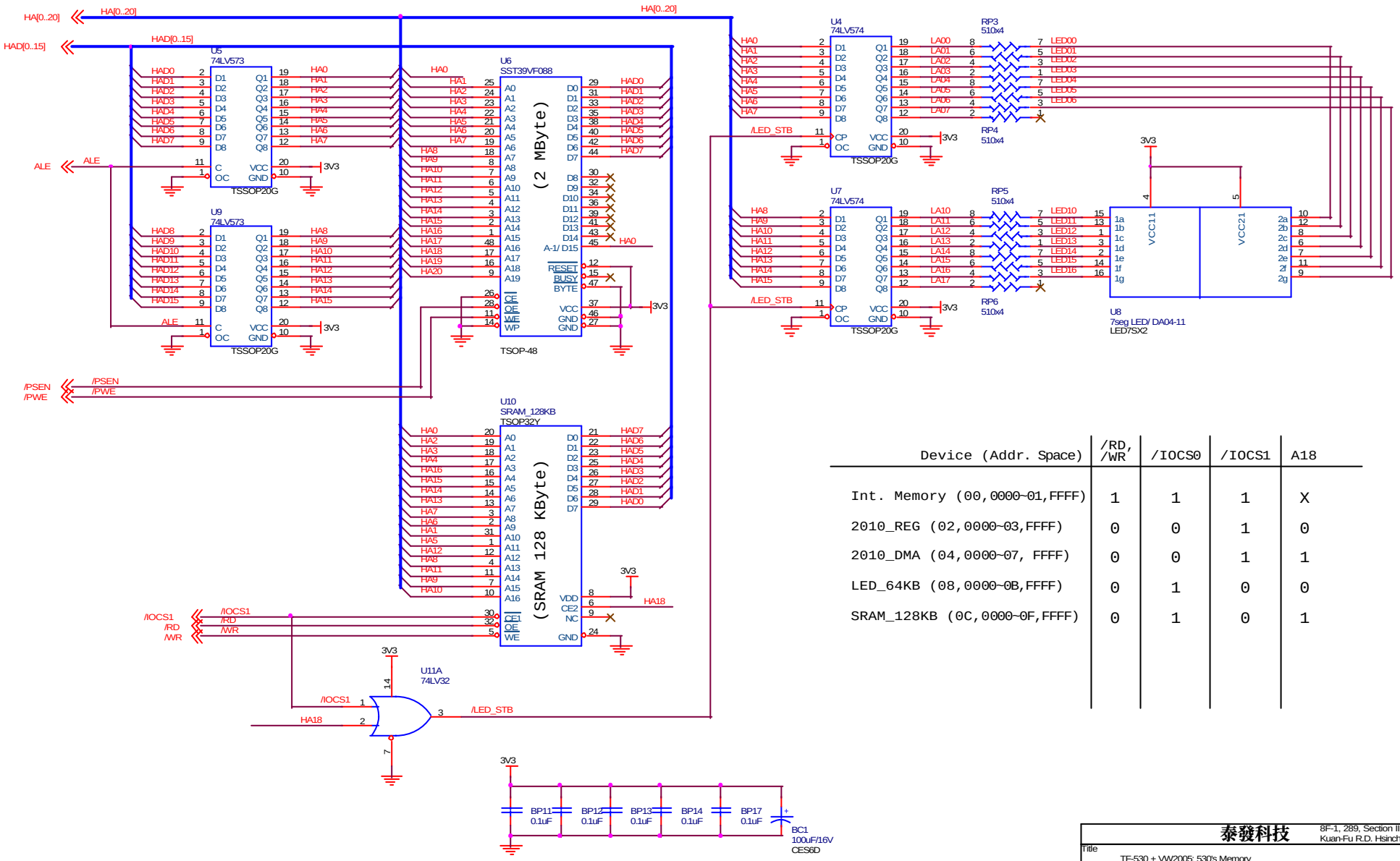


| Device (Addr. Space) | /RD, /WR | /IOCS0 | /IOCS1 | A18 |
|---|---|---|---|---|
| Int. Memory (00,0000~01,FFFF) | 1 | 1 | 1 | X |
| 2010_REG (02,0000~03,FFFF) | 0 | 0 | 1 | 0 |
| 2010_DMA (04,0000~07, FFFF) | 0 | 0 | 1 | 1 |
| LED_64KB (08,0000~0B,FFFF) | 0 | 1 | 0 | 0 |
| SRAM_128KB (0C,0000~0F,FFFF) | 0 | 1 | 0 | 1 |

| | | |
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| Title: TF-530 + VW2005: 530's Memory | | |
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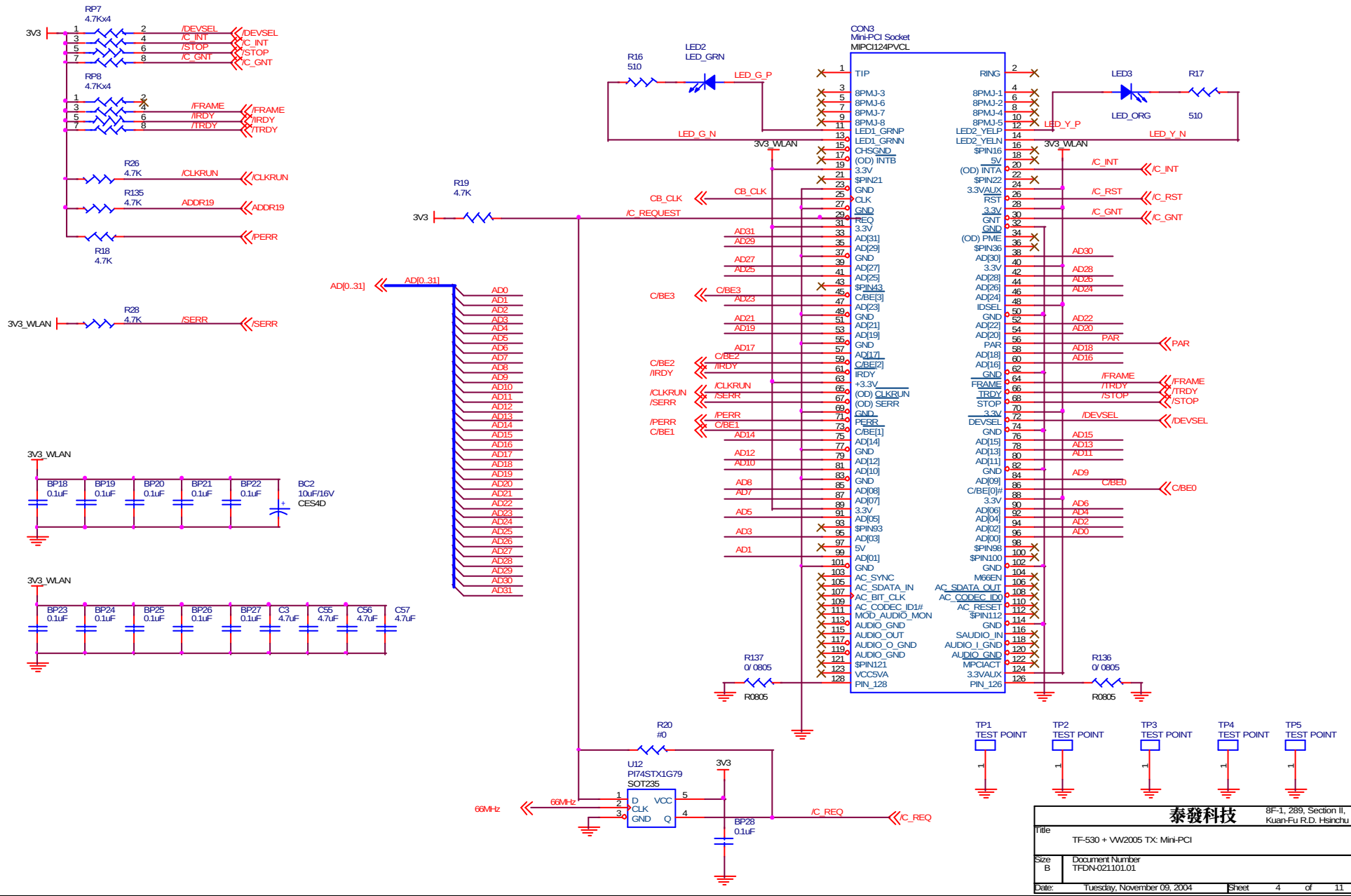


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| | | |
|---|---|---|
| Title | TF-530 + VW2005 TX: Mini-PCI | |
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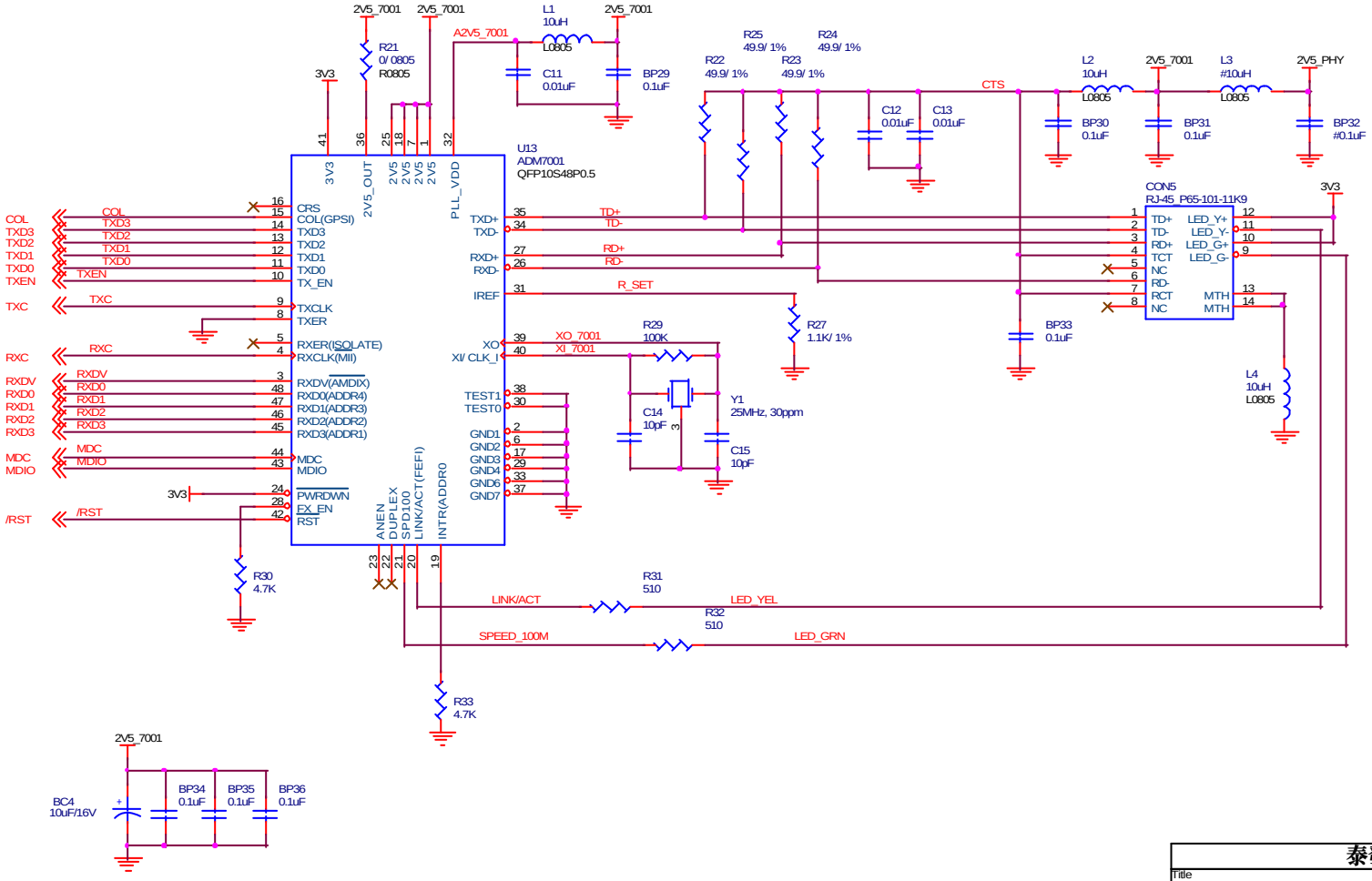


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| Title: TF-530+ VW2005 TX: LAN PHY | | |
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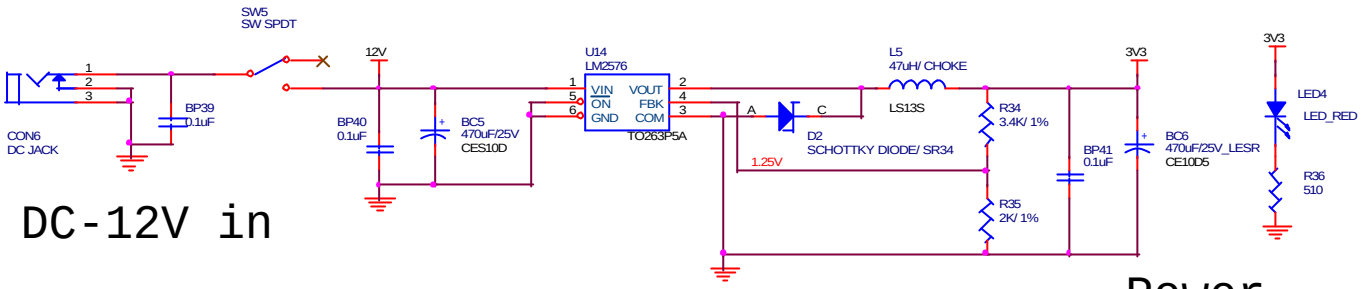
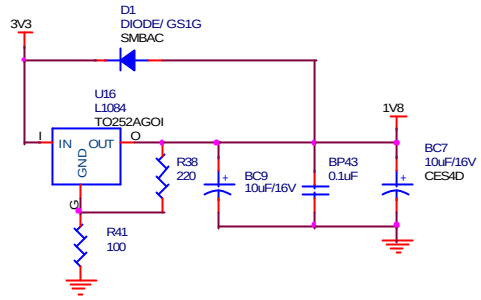


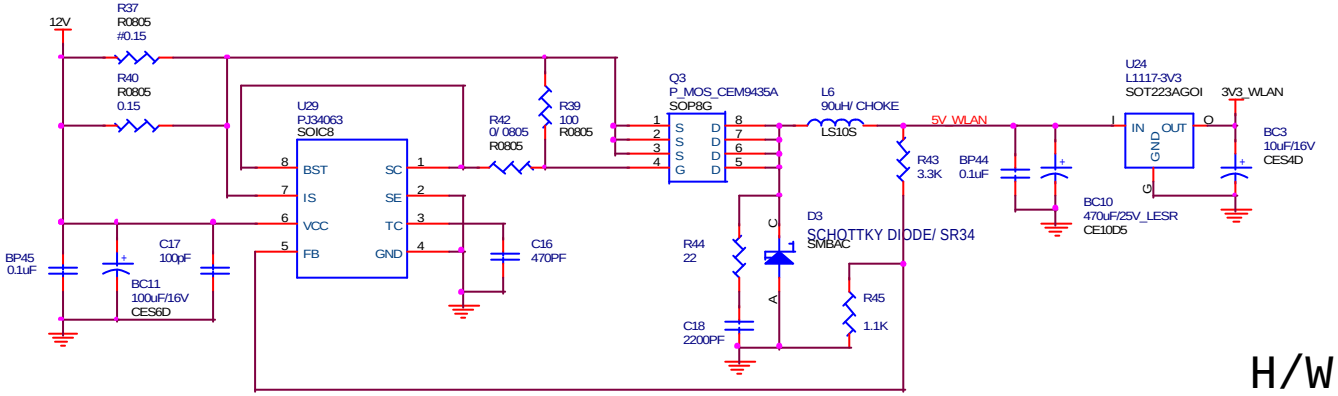

DC-12V in

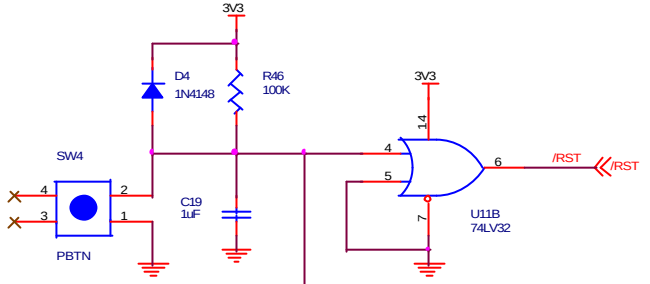
12V-> 3V3(1.5A)

Power Indicator

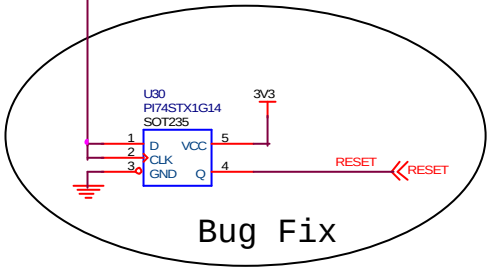



3V3-> 1V8, 1A (VW2010 & TF-530 Core)

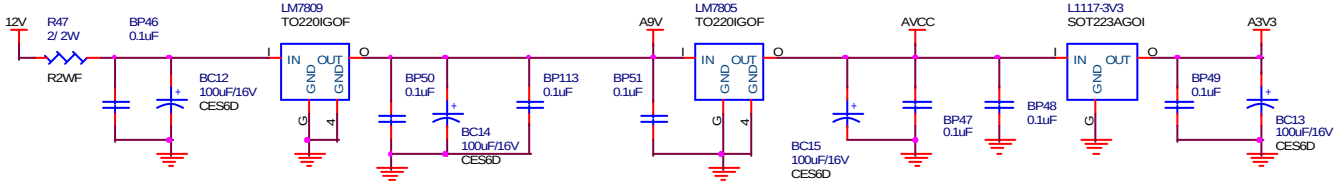



H/W Reset




Bug Fix

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| Title: TF-530 + VW20005: Power & Module Header | | |
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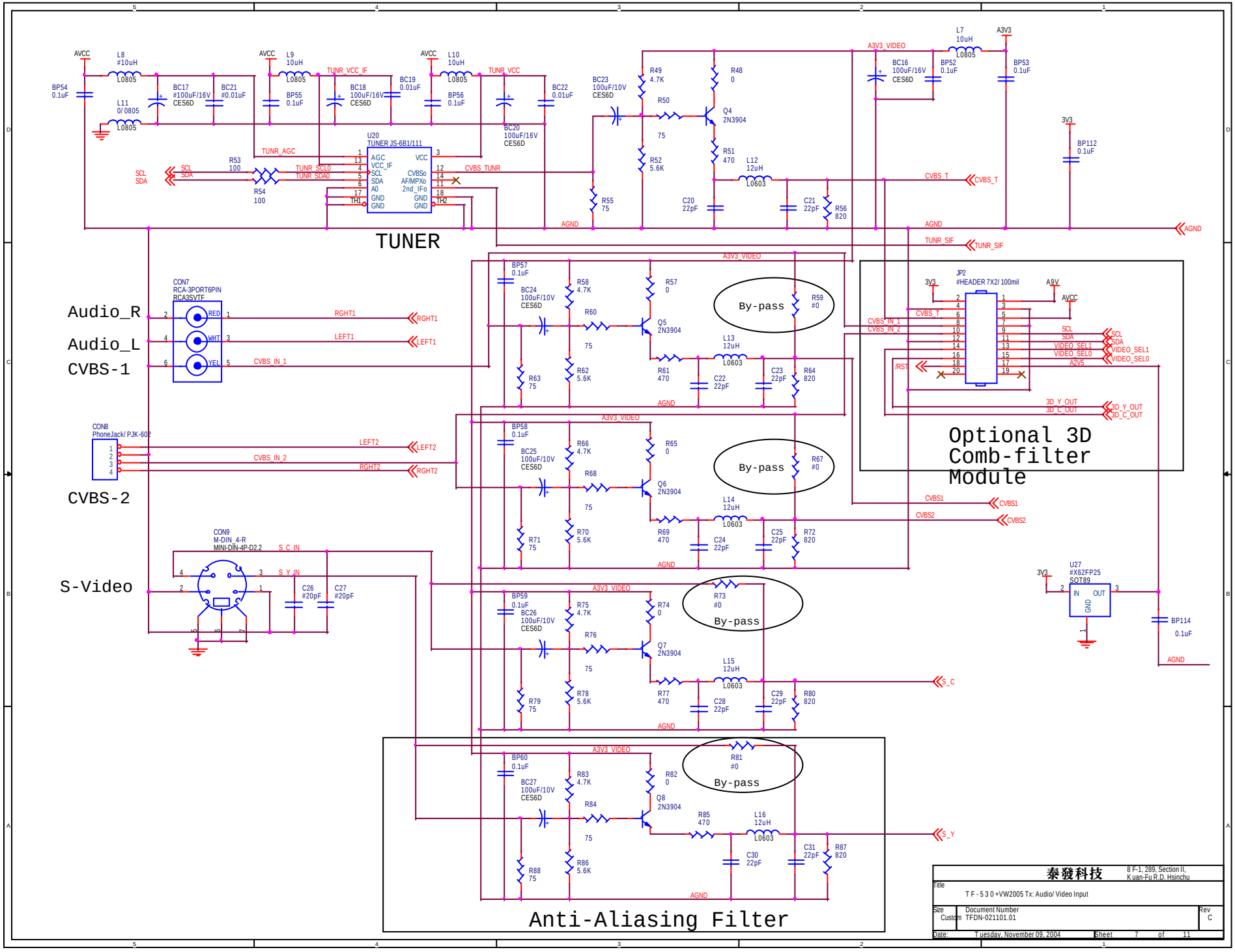
TUNER
Audio_R
Audio_L
CVBS-1
CVBS-2
S-Video
Optional 3D Comb-filter Module
By-pass
Anti-Aliasing Filter
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Title
T F - 5 3 0 +VW2005 Tx: Audio/ Video Input
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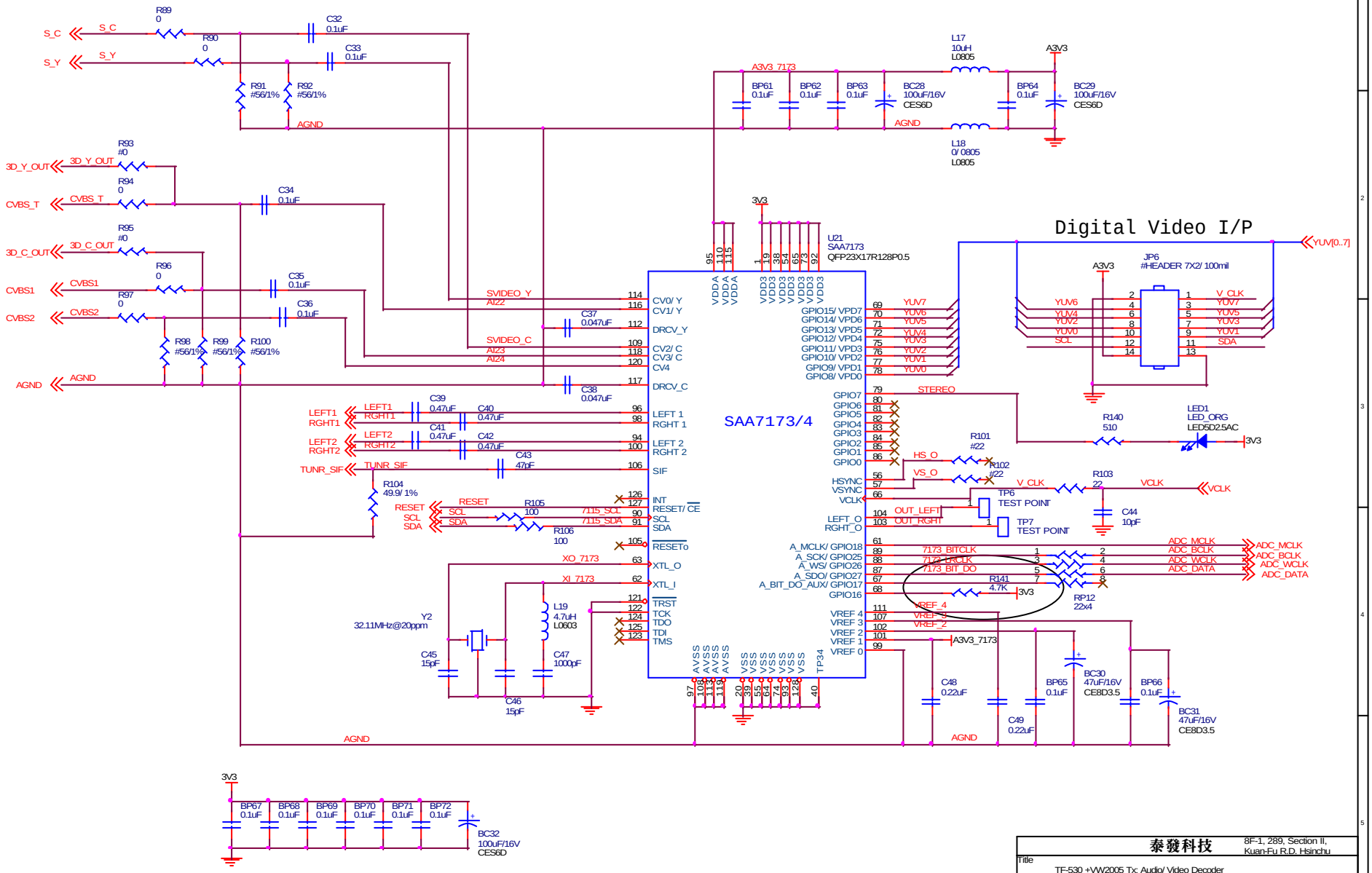
Digital Video I/P
SAA7173/4
U21
SAA7173
QFP23X17R128P0.5
S_C
S_Y
3D_Y_OUT
CVBS_T
3D_C_OUT
CVBS1
CVBS2
AGND
3V3
A3V3
A3V3_7173
YUV[0..7]
JP6
#HEADER 7X2/ 100mil
V_CLK
SDA
SCL
STEREO
LED1
LED_ORG
LED5D2.5AC
HS_O
VS_O
VCLK
OUT_LEFT
OUT_RGHT
TP6
TEST POINT
TP7
TEST POINT
7173_BITCLK
7173_BCLK
7173_BIT_DO
ADC_MCLK
ADC_BCLK
ADC_WCLK
ADC_DATA
RP12
22x4
SVIDEO_Y
SVIDEO_C
LEFT1
RGHT1
LEFT2
RGHT2
TUNR_SIF
RESET
7115_SCL
7115_SDA
XO_7173
XI_7173
Y2
32.11MHz@20ppm
L17
10uH
L0805
L18
0/ 0805
L0805
L19
4.7uH
L0603
BC28
100uF/16V
CES6D
BC29
100uF/16V
CES6D
BC30
47uF/16V
CE8D3.5
BC31
47uF/16V
CE8D3.5
BC32
100uF/16V
CES6D
TP34
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TF-530 +VW2005 Tx: Audio/ Video Decoder
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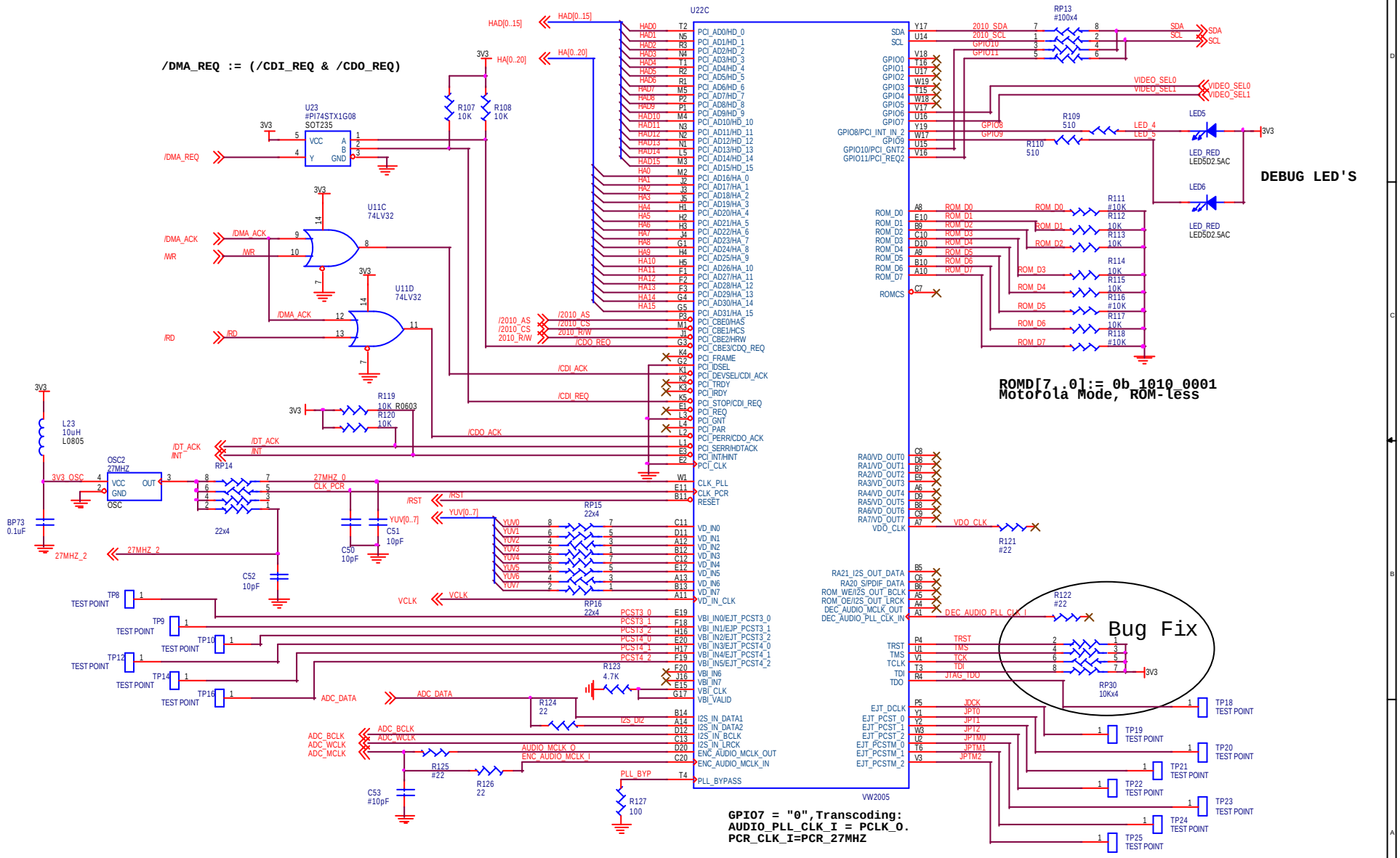


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| Title: T F - 5 3 0 + VW2005: Host I/F (part A) | | |
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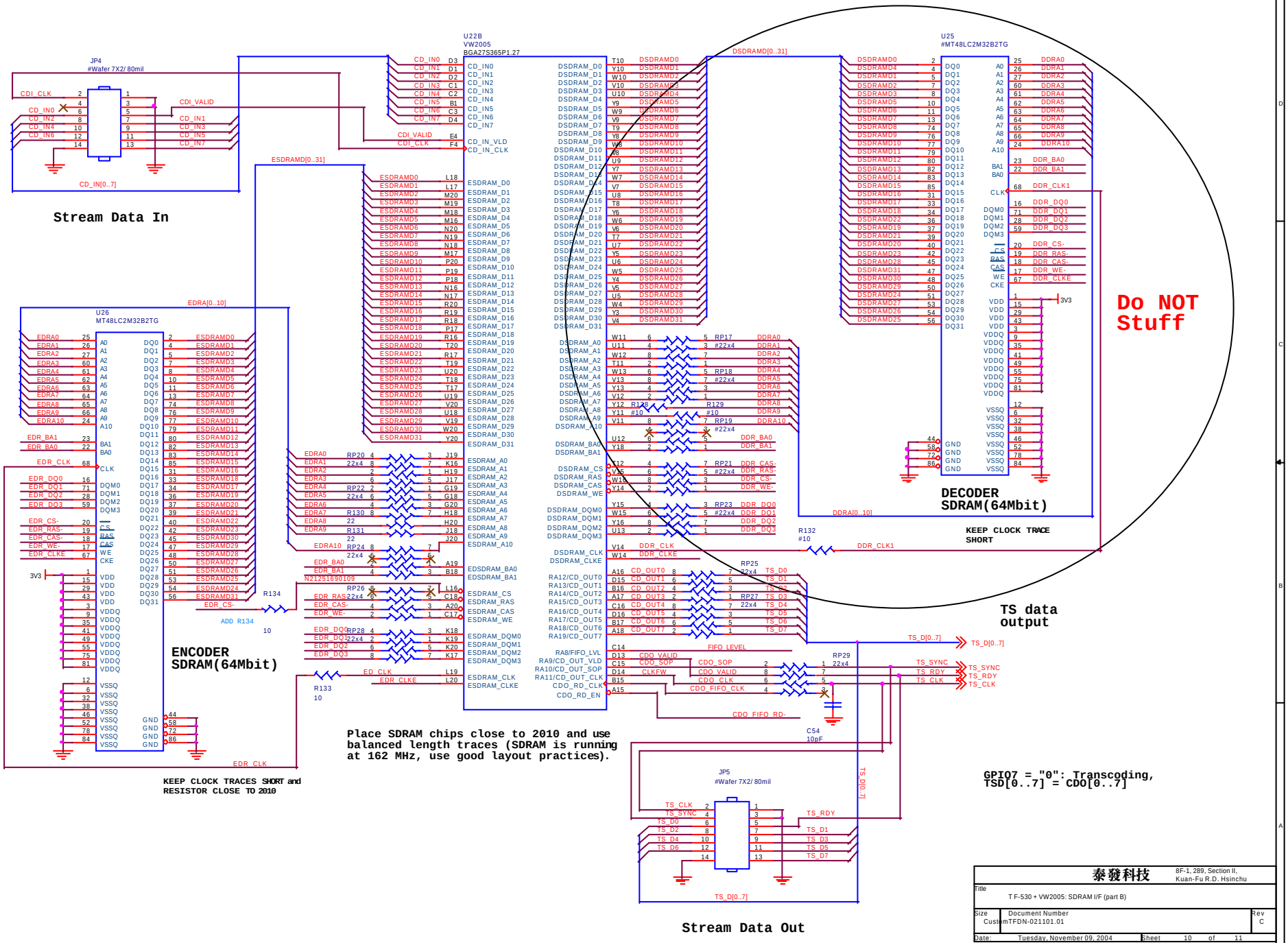
JP4
#Wafer 7X2/ 80mil
CDI_CLK
CD_IN0
CD_IN2
CD_IN4
CD_IN6
CDI_VALID
CD_IN1
CD_IN3
CD_IN5
CD_IN7
CD_IN[0..7]
Stream Data In
U22B
VW2005
BGA27S365P1.27
CD_IN0
CD_IN1
CD_IN2
CD_IN3
CD_IN4
CD_IN5
CD_IN6
CD_IN7
CDI_VALID
CDI_CLK
CD_IN_VLD
CD_IN_CLK
ESDRAMD[0..31]
DSDRAM[0..31]
U25
#MT48LC2M32B2TG
U26
MT48LC2M32B2TG
EDRA[0..10]
EDR_BA1
EDR_BA0
EDR_CLK
EDR_DQ0
EDR_DQ1
EDR_DQ2
EDR_DQ3
EDR_CS-
EDR_RAS-
EDR_CAS-
EDR_WE-
EDR_CLKE
3V3
R134
ADD R134
10
EDR_CS-
EDR_CLK
ENCODER
SDRAM(64Mbit)
KEEP CLOCK TRACES SHORT and
RESISTOR CLOSE TO 2010
Place SDRAM chips close to 2010 and use
balanced length traces (SDRAM is running
at 162 MHz, use good layout practices).
R133
10
ED_CLK
EDR_CLKE
DECODER
SDRAM(64Mbit)
KEEP CLOCK TRACE
SHORT
DDRA[0..10]
DDR_CLK1
R132
#10
Do NOT
Stuff
TS data
output
TS_D[0..7]
TS_SYNC
TS_RDY
TS_CLK
FIFO_LEVEL
CDO_VALID
CDO_SOP
CDO_CLK
CDO_FIFO_CLK
CDO_FIFO_RD-
C54
10pF
JP5
#Wafer 7X2/ 80mil
TS_CLK
TS_SYNC
TS_D0
TS_D2
TS_D4
TS_D6
TS_RDY
TS_D1
TS_D3
TS_D5
TS_D7
Stream Data Out
GPIO7 = "0": Transcoding,
TSD[0..7] = CDO[0..7]
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Title
T F-530 + VW2005: SDRAM I/F (part B)
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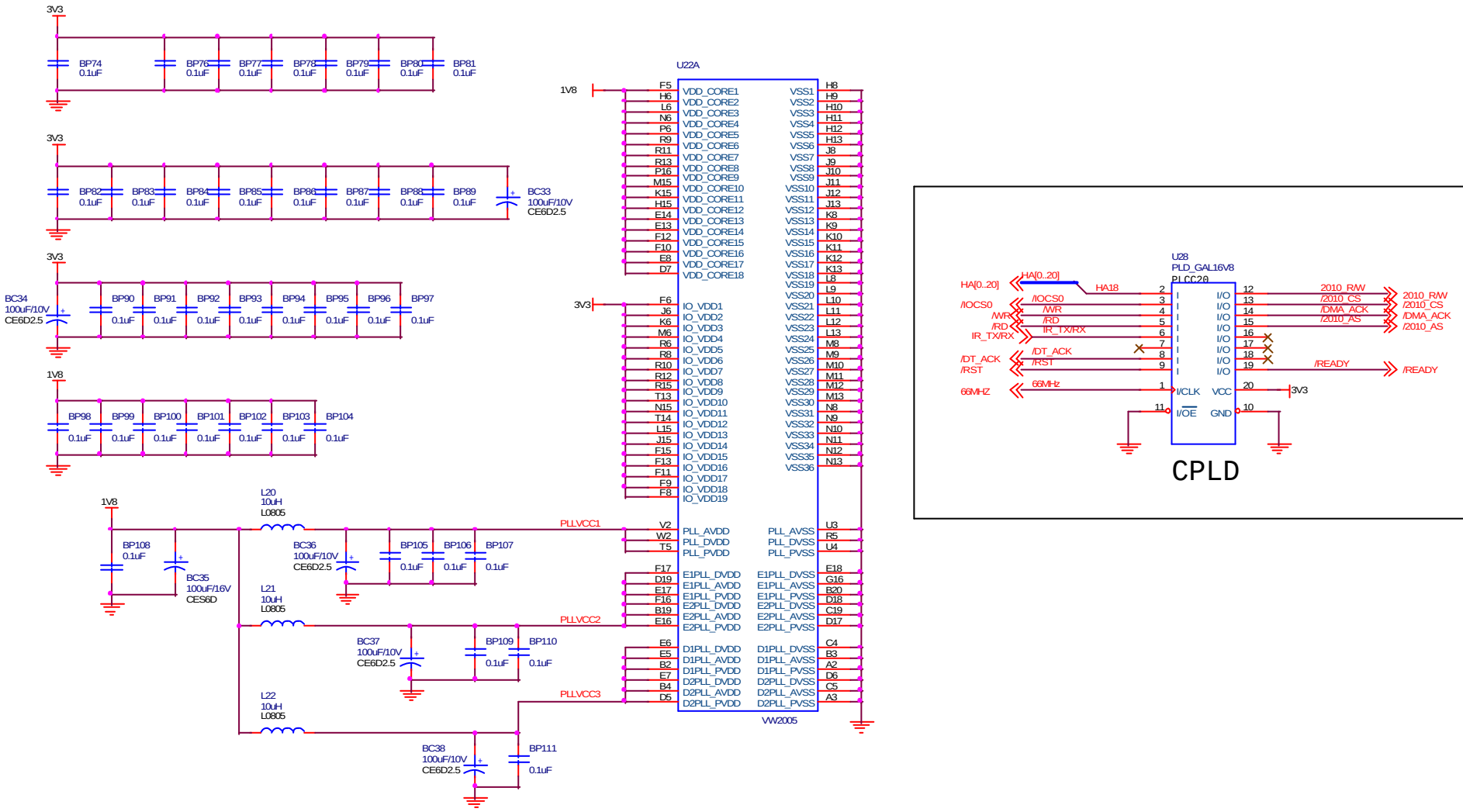


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